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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,495	11/21/2003	David J. Alcoe	EN9-99-073US2	3023

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EXAMINER	
HOGANS, DAVID L	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,495	ALCOE ET AL.	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-21-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to the Transmittal of New Application filed on November 11, 2003.

Status of Claims

Claims 15-26 are pending. Claims 1-14 and 27-29 are cancelled.

Priority

1. This application appears to be a division of Application No. 09/571,611, filed May 15, 2000. A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The divisional application should set forth only that portion of the earlier disclosure which is germane to the invention as claimed in the divisional application.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on November 21, 2003, is in compliance with the provisions of 37 CFR 1.97, and accordingly, has been considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by 5,557,844 to Bhatt et al.

In reference to Claim 15, Bhatt et al. teaches:

- providing a substrate (3), having a plated through hole (7a and 7b) therein; (See Figure 1 and columns 2-7 lines 15-35)
- depositing a redistribution layer (5) on a first and a second surface of the substrate; (See Figure 1 and columns 2-7 lines 15-35) and
- forming a via within the redistribution layer (noting PCB 1's connection to the PTH's), selectively positioned over and electrically contacting (21) the plated through hole (7a or 7b) (See Figure 1 and columns 2-7 lines 15-35)

The Examiner notes that Merriam-Webster's Collegiate Dictionary (2001), Tenth Edition, defines over as "above". Additionally, neither "over" or "above" requires one element to be positioned in contact with or in direct alignment with the other element.

In reference to Claim 16, Bhatt et al. teaches:

- forming a chip connection pad in the via (See Figure 1 and columns 2-7 lines 15-35; specifically noting connection sites with PCB 1 and C4 contacts)

In reference to Claim 17, Bhatt et al. teaches:

- drilling a hole through the substrate; (See Figure 1 and columns 2-7 lines 15-35)

- cleaning the hole; (See Figure 1 and columns 2-7 lines 15-35) and
- forming a conductive layer on an interior surface of the hole (See Figure 1 and columns 2-7 lines 15-35)

In reference to Claim 18, Bhatt et al. teaches:

- filling the plated through hole with a reinforcing material (See Figure 1 and columns 2-7 lines 15-35; noting fill compostion)

In reference to Claim 19, Bhatt et al. teaches:

- wherein the reinforcing material comprises an electrically conductive material (See Figure 1 and columns 2-7 lines 15-35)

In reference to Claim 20, Bhatt et al. teaches:

- wherein the step of depositing the redistribution layer is performed using a lamination process (See Figure 1 and columns 2-7 lines 15-35; noting column 7)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 15-20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,000,130 to Chang et al. in view of Bhatt et al.

Claim 15

Chang et al. teaches providing a substrate (14), having a plated through hole (20) therein; depositing a redistribution layer (12) on a first surface of the substrate; and forming a via (42) within the redistribution layer (5), selectively positioned over and electrically contacting (26 and 49, 50, 51) the plated through hole (20). (See Figures 1-6 and columns 2-6 lines 30-42)

Chang et al. fails to explicitly teach wherein the redistribution layer is on a first and second surface of the substrate.

However, Bhatt et al., in Figure 1, teaches wherein the redistribution layer is on a first and second surface of the substrate.

It would have been obvious to one of ordinary skill in the art to modify Chang et al. by incorporating wherein the redistribution layer is on a first and second surface of the substrate, as taught by Bhatt et al., to increase surface circuitization on the printed circuit board (PCB), thereby increasing the number of surface mounted devices.

Claim 16

Incorporating all arguments of Claim 15 and noting that Chang et al. teaches forming a chip connection pad (44, 46, 49, 50 and 51) in the via (42). (See Figure 1)

Claim 17

Incorporating all arguments of Claim 15 and noting that Chang et al. fails to explicitly teach drilling a hole through the substrate, cleaning the hole and forming a conductive layer on an interior surface of the hole.

However, Bhatt et al., in Figure 1 and columns 2-7 lines 15-35, teaches drilling a hole through the substrate, cleaning the hole and forming a conductive layer on an interior surface of the hole.

It would have been obvious to one of ordinary skill in the art to modify Chang et al. by incorporating drilling a hole through the substrate, cleaning the hole and forming a conductive layer on an interior surface of the hole, as taught by Bhatt et al., to remove any debris that could deleteriously affect the adhesive qualities of the conductive layer to the via.

Claim 18

Incorporating all arguments of Claim 15 and noting that Chang et al. fails to explicitly teach filling the plated through hole with a reinforcing material.

However, Bhatt et al., in Figure 1 and columns 2-7 lines 15-35, teaches filling the plated through hole with a reinforcing material.

It would have been obvious to one of ordinary skill in the art to modify Chang et al. by incorporating filling the plated through hole with a reinforcing material, as taught by Bhatt et al., to provide enhanced structural quality by removing void spaces and to provide another medium (i.e. – the filler) with similar thermal expansion properties to the subcomposite, thereby reducing stress in the void areas.

Claim 19

Incorporating all arguments of Claim 15 and noting that Chang et al. fails to explicitly teach wherein the reinforcing material comprises an electrically conductive material.

However, Bhatt et al., in Figure 1 and columns 2-7 lines 15-35, teaches wherein the reinforcing material comprises an electrically conductive material.

It would have been obvious to one of ordinary skill in the art to modify Chang et al. by incorporating wherein the reinforcing material comprises an electrically conductive material, as taught by Bhatt et al., to provide an additional source of conduction within the via to enhance transmission of electrical signals.

Claim 20

Incorporating all arguments of Claim 15 and noting that Chang et al. fails to explicitly teach wherein the step of depositing the redistribution layer is performed using a lamination process.

However, Bhatt et al., in Figure 1 and columns 2-7 lines 15-35, teaches wherein the step of depositing the redistribution layer is performed using a lamination process.

It would have been obvious to one of ordinary skill in the art to modify Chang et al. by incorporating wherein the step of depositing the redistribution layer is performed using a lamination process, as taught by Bhatt et al., to remove air that resides in between layers that could cause a void formation.

Claim 25

Incorporating all arguments of Claim 15 and noting that Chang et al. teaches wherein the redistribution layer comprises a fatigue resistant dielectric material. (See column 6 lines 17-30)

7. Claims 21, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,557,844 to Bhatt et al. in view of Kresge et al.

Claim 21

Incorporating all arguments of Claim 15 and noting that Bhatt et al. fails to explicitly teach providing a substrate with a ground plane; forming a first pair of signal planes within the substrate; forming a first pair of power cores within the substrate; forming a second pair of signal planes within the substrate; and forming a second pair of power cores within the substrate.

However, Kresge et al., in Figures 1-9 and columns 6-10 lines 47-25, teaches providing a substrate (12) with a ground plane (22); forming a first pair of signal planes (18) within the substrate; forming a first pair of power cores (20) within the substrate; forming a second pair of signal planes (18) within the substrate; and forming a second pair of power cores (20) within the substrate.

It would have been obvious to one of ordinary skill in the art to modify Bhatt et al. by incorporating providing a substrate with a ground plane; forming a first pair of signal planes within the substrate; forming a first pair of power cores within the substrate; forming a second pair of signal planes within the substrate; and forming a second pair of power cores within the substrate, as taught by Kresge et al., to provide additional circuitry to support an increase in surface mounted devices on the PCB.

Claim 23

Incorporating all arguments of Claims 15 and 21 and noting that Bhatt et al. fails to explicitly teach wherein the second pair of power cores are directly underneath and electrically connected to portions of the redistribution layer.

However, Kresge et al., in Figures 1-9 and columns 6-10 lines 47-25, teaches wherein the second pair of power cores (20) are directly underneath and electrically connected to portions of the redistribution layer.

It would have been obvious to one of ordinary skill in the art to modify Bhatt et al. by incorporating wherein the second pair of power cores are directly underneath and electrically connected to portions of the redistribution layer, as taught by Kresge et al., to reduce attenuation of the voltage signal in the power lines and thereby create uniform voltage levels.

Claim 24

Incorporating all arguments of Claims 15 and 21 and noting that Bhatt et al. fails to explicitly teach wherein the second pair of power cores further includes a top surface metallurgy and a bottom surface metallurgy.

However, Kresge et al., in Figures 1-9 and columns 6-10 lines 47-25, teaches wherein the second pair of power cores (20) further includes a top surface metallurgy (connections to vias 24) and a bottom surface metallurgy (connections to vias 48).

It would have been obvious to one of ordinary skill in the art to modify Bhatt et al. by incorporating wherein the second pair of power cores further includes a top surface metallurgy and a bottom surface metallurgy, as taught by Kresge et al., to provide electrical current to surface mounted devices through interconnects and chip connection pads.

8. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,557,844 to Bhatt et al. in view of Kresge et al. further n view of 6,388,208 to Kiani et al.

Incorporating all arguments of Claims 15 and 21 and noting that Bhatt et al. and Kresge et al. fail to explicitly teach wherein the first and second pair of signal planes are controlled impedance circuitry.

However, Kiani et al., in Figure 1 and columns 3-4 lines 45-16, teaches wherein the first and second pair of signal planes are controlled impedance circuitry.

It would have been obvious to one of ordinary skill in the art to modify Bhatt et al. and Kresge et al. by incorporating wherein the first and second pair of signal planes are controlled impedance circuitry, as taught by Kiani et al., to provide uniform voltage within the signal circuitry.

9. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over 6,000,130 to Chang et al. in view of 5,557,844 to Bhatt et al. further in view of 5,574,630 to Kresge et al.

Incorporating all arguments of Claim 15 and noting that Chang et al. and Bhatt et al. fail to explicitly teach providing a substrate with a ground plane; forming a first pair of signal planes within the substrate; forming a first pair of power cores within the substrate; forming a second pair of signal planes within the substrate; and forming a second pair of power cores within the substrate.

However, Kresge et al., in Figures 1-9 and columns 6-10 lines 47-25, teaches providing a substrate (12) with a ground plane (22); forming a first pair of signal planes (18) within the substrate; forming a first pair of power cores (20) within the substrate; forming a second pair of signal planes (18) within the substrate; and forming a second pair of power cores (20) within the substrate.

It would have been obvious to one of ordinary skill in the art to modify Chang et al. and Bhatt et al. by incorporating providing a substrate with a ground plane; forming a first pair of signal planes within the substrate; forming a first pair of power cores within the substrate; forming a second pair of signal planes within the substrate; and forming a second pair of power cores within the substrate, as taught by Kresge et al., to provide additional circuitry to support an increase in surface mounted devices on the PCB.

10. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,557,844 to Bhatt et al. in view of 5,929,729 to Swarup.

Incorporating all arguments of Claim 15 and noting that Bhatt et al. fails to explicitly teach providing a buried plated trough hole in the substrate.

However, Swarup, in Figures 3B, 5B and 6B and columns 7-12 lines 30-22, teaches providing a buried plated trough hole in the substrate.

It would have been obvious to one of ordinary skill in the art to modify Bhatt et al. by incorporating providing a buried plated trough hole in the substrate, as taught by Swarup, to provide an interconnection between two adjacent metal layers.

11. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over 6,000,103 to Chang et al. in view of 5,557,844 to Bhatt et al. further in view of 5,929,729 to Swarup.

Incorporating all arguments of Claim 15 and noting thatching et al. and Bhatt et al. fails to explicitly teach providing a buried plated trough hole in the substrate.

However, Swarup, in Figures 3B, 5B and 6B and columns 7-12 lines 30-22, teaches providing a buried plated trough hole in the substrate.

It would have been obvious to one of ordinary skill in the art to modify chang et al. and Bhatt et al. by incorporating providing a buried plated trough hole in the substrate, as taught by Swarup, to provide an interconnection between two adjacent metal layers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (571) 272-1691. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER

DH